

**IN THE CLAIMS:**

1. (Currently Amended) A package ~~for~~ containing a semiconductor element comprising:

a housing ~~having a recess portion for~~ containing a semiconductor element, said housing having two primary side walls that are perpendicular to each other; and

a pair of positioning holes and a pair of attaching holes respectively provided at opposed side portions of said housing,

wherein a line between said pair of positioning holes and a line between said pair of attaching holes intersect with each other substantially at a center of said package and further wherein the line between the positioning holes is skewed with respect to each of the two primary side walls of the housing and the line between the attaching holes is skewed with respect to each of the primary side walls such that the line between the positioning holes and the line between the attaching holes are each neither parallel nor perpendicular to either of the primary side walls.

2. (Original) The package according to claim 1:

wherein said semiconductor element is a solid-state imaging element.

3. (Currently Amended) A semiconductor device comprising:

a semiconductor element;

a housing ~~having a recess portion for~~ containing said semiconductor element, said housing having two primary side walls that are perpendicular to each other; and

a pair of positioning holes and a pair of attaching holes respectively provided at opposed side portions of said housing;

wherein a line between the pair of positioning holes and a line between said pair of attaching holes intersect with each other substantially at a center of said package and further wherein the line between the positioning holes is skewed with respect to each of the primary side walls of the housing and the line between the attaching holes is skewed with respect to each of the primary side walls such that the line between the positioning holes and the line between the attaching holes are each neither parallel nor perpendicular to either of the primary side walls.

4. (Original) The semiconductor device according to claim 3,  
wherein said semiconductor element is a solid-state imaging element.

5. (Currently Amended) A semiconductor device comprising:

a semiconductor element;

a housing ~~having a recess portion for~~ containing said semiconductor element, said housing having two primary side walls that are perpendicular to each other;

a pair of attaching holes provided at opposed side portions of said housing at a surface of said package; and

a transparent member for sealing said semiconductor element in ~~said a~~ recess portion;

wherein said surface of said housing is made to be higher than a top surface of said transparent member, and further wherein a line between the pair of positioning holes and a line between said pair of attaching holes intersect with each other substantially at a center of said package and further wherein the line between the positioning holes is skewed with

respect to each of the primary side walls of the housing and the line between the attaching holes is skewed with respect to each of the primary side walls such that the line between the positioning holes and the line between the attaching holes are each neither parallel nor perpendicular to either of the primary side walls.

6. (Original) The semiconductor device housing according to claim 5,  
wherein said semiconductor element is a solid-state imaging element.

### **REMARKS**

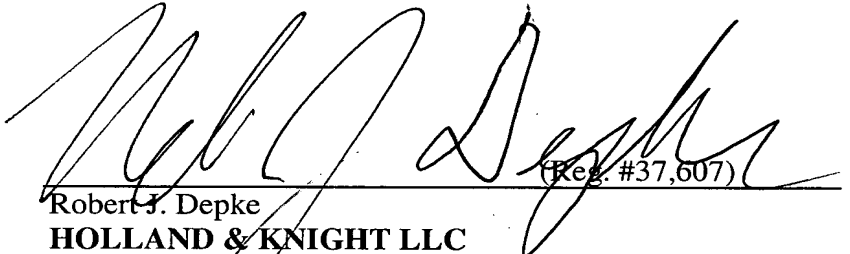
In response to the final office action dated June 3, 2003, Applicant has submitted a Request for Continued Examination and the instant amendment which Applicant submits overcomes the rejections set forth by the Examiner in the referenced final office action. In regard to the rejections set forth under 35 USC section 112, second paragraph, Applicant has modified claims in order to more clearly define the invention. Applicant submits that the modified claims overcome the Examiner's rejections under 35 USC section 112. Applicant submits that all of the claims now comport with the requirements of section 112 and accordingly, Applicant requests that the Examiner now withdraw these rejections.

Applicant also respectfully requests reconsideration of the prior art rejections set forth under 35 USC sections 102 and 103. Applicant respectfully submits that the prior art references of record, whether considered alone, or in combination, fail to either teach or suggest Applicant's presently claimed invention. More specifically, Applicant has modified the claims to recite that the housing has two primary side walls and that the lines between the positioning holes and the attaching holes are neither perpendicular nor parallel to each of the primary sidewalls.

Applicant submits that the references of record fail to teach or suggest such a structure, Applicant acknowledges the Examiner's reference to the minor sidewall in the Arai reference, United States patent number 5,686,758. However, Applicant notes that this is just a minor notch in the corner of the chip and not the primary sidewall as now recited in the claims of the instant application. Accordingly, Applicants submits that all claims now stand in condition for allowance.

Respectfully submitted,

Date: October 3, 2003

  
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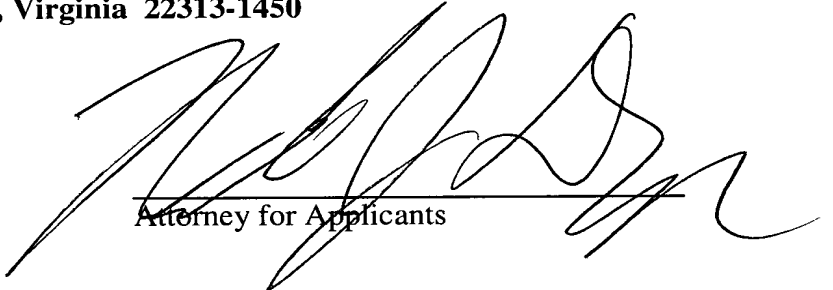
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**CERTIFICATE OF MAILING**

I hereby certify that this correspondence is being deposited with the United States Postal Service as Express Mail No. **ET905260727US**, Post Office to Addressee, on October 3, 2003 in an envelope addressed to:

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